In The Claims:

1. (Currently Amended) A dual processor system, comprising:

(a) a first processor coupled to a system address bus and a data bus; and

(b) a second processor coupled to the system address bus and to the data bus, the second processor comprising a control register having a control register system address, an internal memory partitioned into a plurality of blocks each having a known number of addressable memory locations, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a control word is written into the control register when the first processor places a control word having a burst mode bit, a block identifier and a starting ~~internal~~ address within said identified block, on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting ~~internal~~ address ~~specified in the control word stored in the control register~~, during subsequent data transfer cycles, ~~when the control word has a burst mode bit indicating burst mode~~ when said burst mode is indicated and so long as the first processor asserts the data register system address on the system address bus,

wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting ~~internal~~ address, whereby the subsequent data words are written into the consecutive memory locations independent of a count of words to be exchanged, and

wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting ~~internal~~ address, and the data register reads data words at the consecutive memory locations and

places said data words on the data bus independent of a count of words to be exchanged, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

2 - 3. (Cancelled).

4. (Currently Amended) A processor system, comprising:

(a) a first processor and [a] at least one second processor are intercoupled by a system address bus to select a co-processor in a system having many selectable devices such as other co-processors, a data bus, a chip select line, a read signal line, and a write signal line,

wherein each second processor comprises a control register having a control register system address, an internal memory, partitioned into a plurality of blocks, each having a known number of consecutive memory addresses, a data register having a data register system address ~~and~~ coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a control word is written into the control register when the first processor places a control word having a burst mode bit, a block identifier, and a starting ~~internal~~ address on the data bus and asserts the control register system address on the system address bus; and

~~at least one~~ wherein the internal address generator of a selected one of said second ~~processor~~ processors ~~enters a burst mode in which the internal address generator selects one or more consecutive~~ determines a memory ~~blocks~~ address of the internal memory, starting at the starting ~~internal~~ address within the selected block and increments said determined memory address ~~specified in the control word stored in the control register,~~ during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode, said selected second processor incrementing said determined memory address independent of a number of words to be exchanged so long as said first processor asserts the data register system address on the system address bus. ~~and~~

~~wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal~~

~~address generator selects one or more consecutive memory blocks of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the one or more consecutive memory blocks.~~

5. (Currently Amended) A processor system, comprising:

(a) a first processor and a least one second processor are intercoupled by a system address bus to select a co-processor in a system having many selectable devices such as other co-processors, a data bus, a chip select line, a read signal line, and a write signal line, wherein each second processor comprises a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a control word is written into the control register when the first processor places a control word having a burst mode bit and a starting ~~internal~~ address on the data bus and asserts the control register system address on the system address bus; and

at least one second processor enters a burst mode in which the internal address generator selects one or more consecutive memory blocks of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles <u>independent of a number of words to be exchanged</u>, when the control word has a burst mode bit indicating burst mode; and

wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, and the internal address generator selects one or more consecutive memory blocks of the internal memory, starting at the starting ~~internal~~ address <u>independent of a number of words to be exchanged</u>, and the data register reads data words at the one or more consecutive memory blocks and places said data words on the data bus, whereby the subsequent data words are read from the one or more consecutive memory blocks by the first processor.

6. (Original) The dual processor system of claim 1, wherein the second processor is a co-processor.

7. (Previously Amended) The dual processor system of claim 1, wherein:

the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, and the data is transferred from the first processor to a specified location into memory of the second processor during the next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode.

8. (Original) The dual processor system of claim 1, wherein the first processor and second processor are intercoupled by the system address bus to select a co-processor in a system having many selectable devices such as other co-processors, the data bus, a chip select line, a read signal line, and a write signal line.

9. (Cancelled)

10. (Currently Amended) A multiprocessor system comprising a plurality of interconnected processors each having internal memory[;] and an interconnection operable to transfer information contained in data words therebetween [comprised of] comprising:

a system address bus; ~~and~~

a data bus;[,]

a control register means having a control register system address;[,]

a data register means having a data register system address ~~and~~ coupled to the internal memory;[,] and

an internal address generator means coupled to the control register means and to the internal memory, wherein:

a control word is written into the control register means when a first one of the plurality of interconnected processors places a control word having a burst mode bit and a starting ~~internal~~ address on the data bus and asserts the control register system address on the system address bus; and

a second one of a plurality of interconnected processors enters a burst mode when the control word indicates burst mode in which the internal address generator selects consecutive memory locations of the internal memory, independent of a count of words to be transferred, starting at the starting ~~internal~~ address ~~specified in the control word stored in the control register means,~~ during subsequent data transfer cycles, ~~when the control word has a burst mode bit indicating burst mode~~,

wherein, in a write burst mode, the first one of the plurality of interconnected processors asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations, and

wherein, in a read burst mode, the first one of the plurality of interconnected processors asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register means reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first one of the plurality of interconnected processors; and

said second processor remaining in said burst mode only so long as the first processor asserts the data register system address on the system address bus.

11-13. (Cancelled)

14. (Previously Amended) The multiprocessor system of claim 10, wherein one of the plurality of interconnected processors is a co-processor.

15. (Currently Amended) The multiprocessor system of claim 10, wherein one of the plurality of interconnected processors is a first processor and another of the plurality of interconnected processors is a second processor ~~are~~ intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

16. (Currently Amended) The multiprocessor system of claim 10, wherein:

the internal memory comprises ~~a computer readable medium having~~ a plurality of memory blocks wherein data are stored in consecutive locations;

the control word comprises ~~a computer readable medium having~~ a burst mode bit field, and a memory bank field which specifies a selected memory bank of the plurality of memory banks, and ~~a computer readable medium having an internal bank address field which specifies~~ the starting ~~internal~~ bank address within the selected memory bank.